

Claims

1. Apparatus for converting between analogue and digital signals comprising continuous-time sigma-delta conversion means and clock pulse generator apparatus comprising a clock pulse generator (CLK) for generating a train of return-to zero primary clock pulses each having leading and trailing edges defining alternately an active clock phase (ACP) and a non-active clock phase (NACP),

characterised by delay means (14) for producing a train of delayed clock pulses (CLK_D) presenting delayed edges whose timing relative to corresponding edges of said primary clock pulses (CLK) is defined by said delay means, and combining means (15) for producing a train of combined clock pulses (CLK_JF) presenting leading and trailing edges defined alternately by one of said delayed edges and the corresponding edge of the primary clock pulse, so that the active clock phases (ACP) of said combined clock pulses have widths defined by said delay means, the variability of said widths of said active clock phases (ACP) being smaller than the variability of the positions of said leading and trailing edges of said primary clock pulses (CLK), and the widths of said non-active clock phases (NACP) varying as a function of variation in the positions of said primary clock pulses (CLK).

2. Apparatus for converting between analogue and digital signals as claimed in claim 1 wherein said delay means (14) comprises a series of cascaded, substantially identical delay elements (16).
3. Apparatus for converting between analogue and digital signals as claimed in claim 2 wherein said delay means (14) comprises a further series (22) of cascaded delay elements (27) substantially identical to the first said delay elements (16), adjustment means (24, 25, 26) responsive to the delay of said further series (22) relative to a pulse period of said train of primary clock pulses (CLK) for applying an adjustment signal (V_{tune}) to tend to correct the delay of said further series (22) of delay elements relative to a pulse period, said adjustment signal being averaged over a plurality of clock periods, and

means for applying said adjustment signal (V_{tune}) to adjust the delay of the delay elements (16) of said first series (14).

4. Apparatus for converting between analogue and digital signals as claimed in claim 2 or 3 wherein each of said delay elements (16; 27) comprises a respective capacitive element (18), current supply means (17, 19) responsive to an signal input to the delay element for supplying a controlled current to said respective capacitive element, and trigger means responsive to the voltage (20) at said respective capacitive element (18).
5. Apparatus for converting between analogue and digital signals as claimed in any preceding claim, wherein said continuous-time sigma-delta conversion means comprises integration means (2; 10) for integrating a signal (Input) over periods of time defined by said widths of said active clock phases (ACP).
6. Apparatus for converting between analogue and digital signals as claimed in claim 5, wherein said continuous-time sigma-delta conversion means comprises digital-to-analogue converter means (5; 9) whose operation is responsive to said train of combined clock pulses (CLK_JF).
7. Apparatus for converting an analogue signal to a digital signal in accordance with claim 6, wherein said continuous-time sigma-delta conversion means comprises an input for receiving said analogue signal (Input), an output for said digital signal and a feedback loop from said output including said digital-to-analogue converter means (5).
8. Apparatus for converting a digital signal to an analogue signal in accordance with claim 6, wherein said continuous-time sigma-delta conversion means comprises an input for receiving said digital signal (Input) and an output for said analogue signal (V_{out}), said digital-to-analogue converter means (9) being in series between said input and said output.